SPECIFICATION

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METHOD OF RELIABILITY TESTING

Background of Invention

[0001] Reliability testing is carried out to ensure that products are properly designed and assembled by subjecting test structures to stress conditions that accelerate potential failure mechanisms. Failure may be caused by the degradation of a dielectric layer on a semiconducting or conducting substrate in, for example, Metal Oxide (MOS) integrated circuits (ICs). The aggressive scaling of the thickness of the dielectric layer has caused the reliability of increasingly thinner dielectrics to assume greater importance in the reliability testing of semiconductor ICs.

[0002] The degradation of the dielectric layer over time causes it to lose its insulating properties, leading to increases in leakage current that may limit the lifetime of the device. Long-term failure rates are often predicted based on determining the critical breakdown time of the dielectric layer. Referring to Fig. 1, a reliability test is carried out by subjecting a dielectric layer to highly accelerated stress conditions, such as high temperatures or voltages. The leakage current is continuously measured until the first current increase after, for example, time t_0. This current increase may be relatively small as shown in Fig. 1 or could be a large increase that reaches compliance of the power supply. In the first case, which is mostly found in dielectrics thinner than 5.5 nm, the dielectric layer may experience subsequent breakdowns after t_0, which leads to further increases in current. The criterion for determining the critical breakdown time is the first onset of a current increase at time t_0.

[0003] However, the critical breakdown time of the dielectric layer thus defined does not necessarily cause the circuit or device to be inoperable or lose its functionality. For example, it has been observed that a ring oscillator circuit continues to operate even

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after a number of its transistors have undergone a hard gate-oxide breakdown in B. Kaczer et al, "Impact of MOSFET oxide breakdown on digital circuit operation and reliability", IEDM Tech. Digest, pp. 553-556 (2000), which is herein incorporated by reference for all purposes.

[0004] The magnitude of the current (e.g. I_m) after the dielectric breakdown may not be large enough to cause failure. The magnitude of the leakage current is affected by the circuit environment of the device which includes, for example, the drive current or the capacitative loading of the circuit. The tolerance for current increases varies considerably for different circuits and some circuits are less sensitive to the erosion of noise and voltage margins than others. The lifetime projection based on this criterion tends to be very conservative, as it does not take into account the circuit environment of the device in specific applications.

[0005] Hence, as evident from the foregoing discussion, it is desirable to provide a method of reliability testing that is more accurate and relevant to the IC application.

Summary of Invention

[0006] The present invention relates to a method of reliability testing. In accordance with the invention, a critical breakdown resistance of a device is determined, wherein the critical breakdown resistance causes a circuit to fail. The test structure is then subjected to stress conditions. The operating resistance of the test structure is determined repetitively. A critical breakdown time is recorded when the operating resistance is equal or less than the critical breakdown resistance. The reliability of the device is determined from the critical breakdown time.

Brief Description of Drawings

[0007] Fig. 1 shows a graph depicting the change in current over time of a dielectric layer subjected to accelerated stress conditions and the conventional determination of the critical breakdown time;

[0008] Fig. 2 shows a test structure undergoing testing in accordance with one embodiment of the invention;

[0009] Fig. 3 shows a flowchart of the test method in accordance with one embodiment

of the invention; and

[0010] Fig. 4 shows a graph depicting the change in current over time of a dielectric layer subjected to accelerated stress conditions and the determination of the critical breakdown time in accordance with one embodiment of the invention.

Detailed Description

[0011] The invention relates to the reliability testing of semiconductor ICs and components thereof. In accordance with the invention, the method of reliability takes into account the overall design of the circuit to predict the time of failure. The effect of current leakage caused by the breakdown in the dielectric is dependent on the circuit design, as discussed previously. The device may still have a high resistance value after the first breakdown of the dielectric, which will not cause immediate failure of the circuit. In accordance with the invention, the reliability of the device is characterized by a critical breakdown resistance which causes the circuit to fail or lose its functionality.

[0012] The reliability of the device is determined by subjecting test structures to highly accelerated stress conditions. The test structure comprises a semiconducting or conducting substrate and a dielectric layer formed on the substrate. In one embodiment, the substrate comprises metal or silicon. Other types of substrates are also useful. In one embodiment, the dielectric layer comprises an oxide layer. In another embodiment, the dielectric layer comprises oxide-nitride-oxide (ONO) or nitride-oxide (NO). Other types of dielectric layers are also useful. In one embodiment, the test structure includes the actual device or devices (e.g., transistors or capacitors). In another embodiment, the test structure comprises capacitor structures that have about the same dielectric thickness as the actual device. Such capacitor structures may comprise different shapes (e.g., square, rectangle, circle or comb-like), edge types, edge lengths or areas. This invention also applies to other types of test structures. In one embodiment, the test structure is formed adjacent to the actual device on the same chip.

[0013]

Fig. 2 shows a test structure undergoing testing in one embodiment of the invention. The test structure is coupled to a voltage source 201, which provides the

stress voltage that accelerates the breakdown of the test structure. The test structure comprises a dielectric layer 202 grown on a substrate 204. The test structure comprises, for example, a layer of oxide (e.g., silicon oxide) grown on a silicon substrate. In one embodiment, a gate electrode 206 is formed on the oxide layer. The thickness of the dielectric layer is, for example, less than about 3.4nm. The area of the test structure (e.g., capacitor) is typically about 0.01mm^2 or smaller. Other types of test structures with other areas are also useful. In one embodiment, the current through the test structure is monitored during the testing to detect a significant increase in current, which may indicate a dielectric breakdown.

[0014] Fig. 3 shows a flowchart of the test method, in accordance with one embodiment of the invention. The reliability of the device is characterized by its critical breakdown resistance R_c which causes the circuit to fail or lose its functionality. In one embodiment, the critical breakdown resistance R_c of the device is determined by varying the resistance of the device in the actual circuit environment under normal operating conditions until the circuit fails. In one embodiment, the critical breakdown resistance is obtained through circuit simulation of the actual application. Circuit simulation tools such as HSPICE may be used to simulate the circuit. The critical breakdown resistance coincides with the minimum shunt resistance that is required before the performance of the circuit is degraded beyond its specifications. Depending on the circuit environment, the critical breakdown resistance that causes the circuit to fail can be, for example, in the range of 1k Ω to 100k Ω . Other critical breakdown resistance values can also be useful in accordance with different design requirements.

[0015] For example, the circuit environment comprises a word line driver circuit that is used to internally drive word lines in memory ICs. This invention also applies to other types of circuit environment. If the devices (e.g., transistors) in the circuit experience breakdowns, the voltage and current at the word line will deviate from their normal values during operation. However, the resistances of the devices may still be high enough to prevent a substantial deviation in voltage or current, and the circuit may still be functional after the first breakdown or subsequent multiple breakdowns. The tolerance for deviation depends on the sensitivity of the circuit, and may range from 5% to 30%. Other tolerance values can also be useful, depending on different design

requirements. The circuit loses its functionality when the shunt resistance drops a critical breakdown resistance. In one embodiment, the critical breakdown resistances of all the critical devices in the circuit operating under normal conditions are determined using circuit simulation.

[0016] In one embodiment, the operating resistance R of the nth sample of the test structure (Sample_n) is determined under normal operating conditions, wherein n is an integer less than a predefined number of samples N. If the operating resistance R is less than or equal to the critical breakdown resistance R_c, the test is terminated. If the operating resistance is more than the critical resistance, the test structure is subjected to highly accelerated stress conditions. In one embodiment, the stress conditions comprise elevated voltages, currents or temperatures, or a combination thereof. Other types of stress conditions are also useful. In one embodiment, the stress conditions comprise elevated voltages that are about twice the operating voltage. The test structure is subjected to stress for a duration of, for example, 50 to 10000 seconds. Subjecting the test structure to stress for other periods of time is also useful.

[0017] The operating resistance of the test structure under normal operating conditions is repetitively determined after subjecting the test structure to stress. In one embodiment, the operating resistance is determined after a significant change is detected in at least one electrical property of the test structure. In one embodiment, the electrical property comprises current or voltage. Other electrical properties may also be monitored. For example, if a stress voltage is applied, the current I_a is monitored until it is greater than $X(I_{a-1})$, wherein I_a represents the current measurement at time a, I_{a-1} represents the previous current measurement at time (a-1) and X represents the sensitivity factor, $X \geq 1$. The sensitivity factor X is preferably predefined according to the circuit design.

[0018]

Alternatively, the operating resistance (not shown) is determined after a time interval (e.g., 100 seconds). Providing time intervals of other duration is also useful. The time interval can be predefined according to the stress duration. The time interval is preferably small relative to the breakdown time to avoid significant error. In one embodiment, the time interval changes with the stress duration. For example, the time

interval can be defined as a fraction (e.g., 1/100) of the expected stress duration. In one embodiment, a time interval or a change in electrical properties is used to trigger the determination of operating resistance.

[0019] If the operating resistance R is less than or equal to the critical resistance R_c, the critical breakdown time t_n is recorded. In one embodiment, the test procedure is repeated until a predetermined number N of test structure samples is subjected to the same stress and tested. The reliability of the device is then computed from the critical breakdown times of the test samples.

[0020] In one embodiment, the maximum current I_c available after breakdown and the area of the test structure are provided. The maximum current can be estimated assuming ohmic behavior by Ohm's law using the stress voltage and the critical breakdown resistance R_c. In one embodiment, the area of the dielectric layer in the test structure is about the same as the dielectric layer in the actual device. Dielectric layers having areas different from the actual dielectric layer are also useful. A dielectric layer having a smaller area generally has a longer lifetime. A lifetime correction can be made from the test area to the actual area of the dielectric layer in the device using, for example, the Poisson area scaling.

[0021] As shown in Fig. 4, the critical breakdown time t_c may occur only after a series of soft breakdowns following the initial breakdown at time t_0. Hence, the breakdown time thus defined is more relevant to the application, and allows for a more accurate lifetime projection.

[0022] While the invention has been particularly shown and described with reference to various embodiments, it will be recognized by those skilled in the art that modifications and changes may be made to the present invention without departing from the spirit and scope thereof. The scope of the invention should therefore be determined not with reference to the above description but with reference to the appended claims along with their full scope of equivalents.